Low-Power COS/MOS* Transistor Configuration Dual Complemementary Pair Plus Inverter

Monolithic Silicon

CD4007
CD4007D

File No. 349

RCA CD4007 and CD4007D Integrated Circuits are each comprised of three N-Channel and three P-Channel enhancement-type MOS transistors on a single monolithic silicon chip. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits shown in Fig. 2. The CD4007 utilizes a hermetically sealed 14-lead "Flat Pack" ceramic-and-metal package. The CD4007D is identical, electrically and in terminal configuration, with the CD4007D, and is supplied in a 14-lead dual-in-line ceramic and metal package. Both types are operable over the full military temperature range of -55 °C to +125 °C.

FEATURES

- Nanowatt quiescent power dissipation
  P_T = 10nW typ. with 10-volt supply.
- High noise immunity – – 45% of V_{DD} (typ.)
  over full operating temperature range.
- Operation from single positive or negative power
  supply – – 6 to 15-volt range.
- Large fanout capability – –
  >50
- Fixed logic swing independent of system and fanout
  variations – – V_{DD} to V_{SS}
- High input impedance – –
  $10^{12}\Omega$ (typ.)
- Medium speed operation – – average t_{pd} = 35 ns (typ)
  with a 15-pF load.
- Low "1"- and "0"- level output impedance – –
  1000Ω (typ) with 10-volt supply.

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* Complementary-Symmetry Metal-Oxide-Semiconductor.

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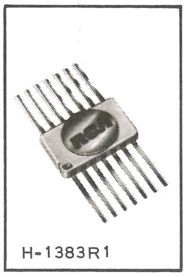
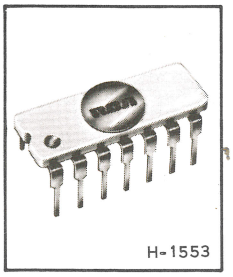
DUAL COMPLEMENTARY PAIR PLUS INVERTER

For Digital Circuits in Aerospace and Airborne Computers, Portable Military Equipment, and Instrumentation and Industrial Control Equipment



CD4007



CD4007D

APPLICATIONS

- Digital equipment where primary design requirements are low power dissipation and/or high noise immunity
- Extremely high-input impedance amplifiers

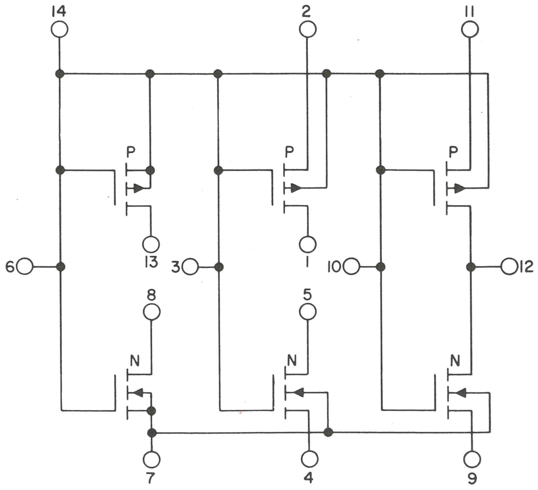


Fig.1 - Schematic diagram for CD4007 and CD4007D.

RCA Electronic Components

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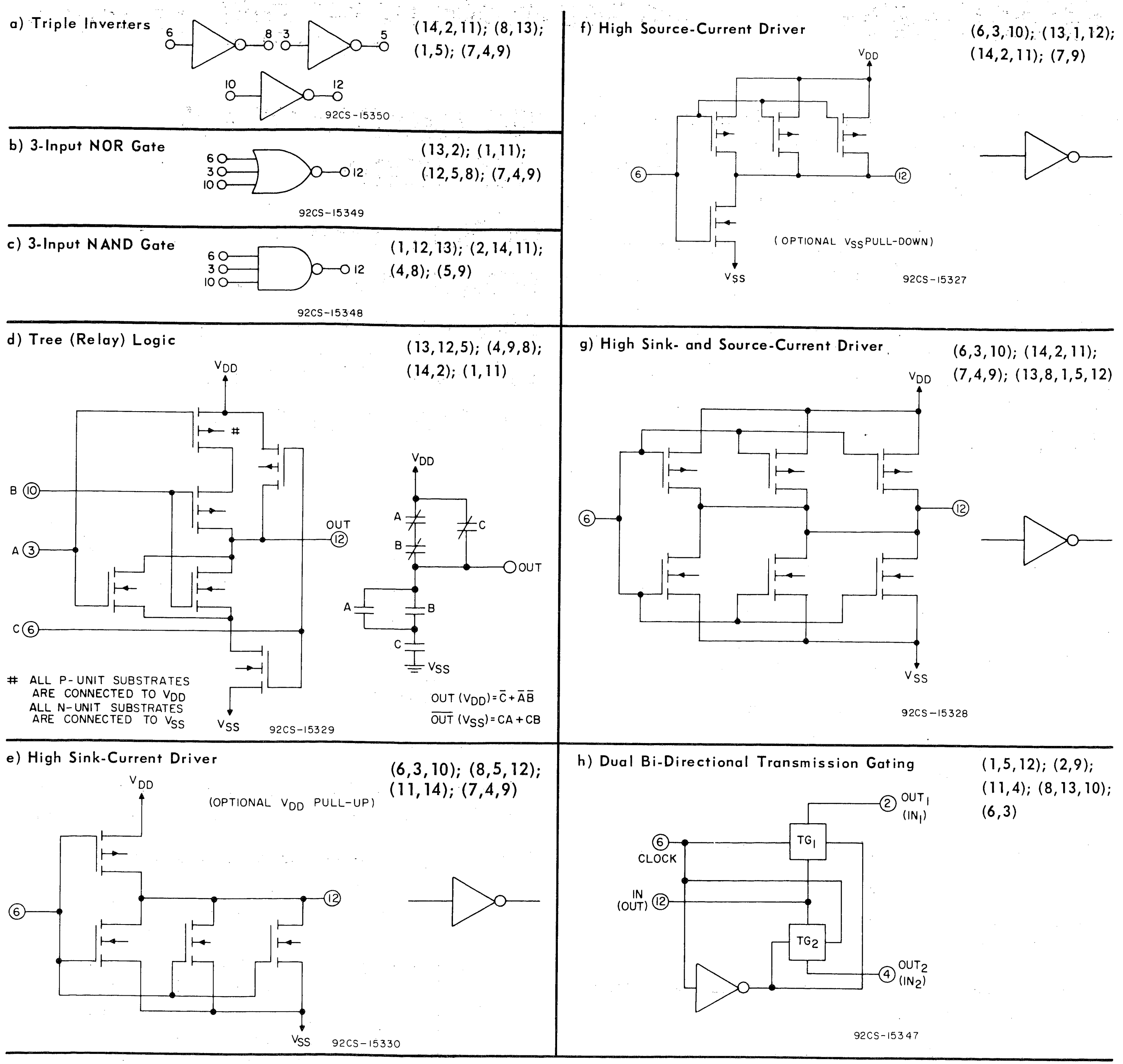
Fig.2 - Sample COS/MOS Logic Circuit Arrangements – Functions, Logic Representations, External Connections● Using CD4007 or CD4007D.*



● Terminal numbers in parentheses are connected together.

* More complex functions possible using multiple packages.

Notes: $V_{SS} \leqq V_{IN} \leqq V_{DD}$; V_{IN} = Terminals 3,6,10.

ABSOLUTE MAXIMUM LIMITS:

STORAGE-TEMPERATURE RANGE . . . -65°C to +150°C
OPERATING-TEMPERATURE RANGE . -55°C to +125°C
DC SUPPLY VOLTAGE (V_{DD} - V_{SS}) . . . . . . +15, -0.5 V
DC CURRENT DRAIN . . . . 10 mA
INPUT TERMINALS 3,6,10 . . . . $V_{SS} \leq V_{IN} \leq V_{DD}$
MINIMUM RECOMMENDED POWER SUPPLY
VOLTAGE (V_{DD} - V_{SS}) . . . . 6 V

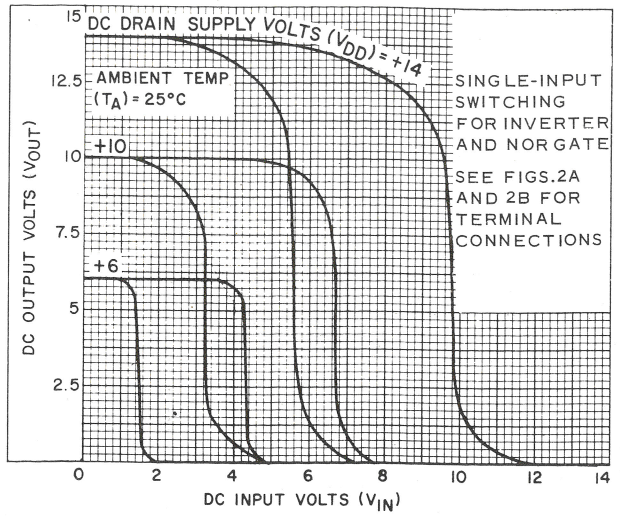
STATIC ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CD4007, CD4007D MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS FIGS.
"0" Output Voltage	V_{OUT}"0"	Fan-out ≦ 10 MOS Gate Loads V_{IN} = 10 V	-	0	0.01	V	3a,3b,3c,3d,3e
"1" Output Voltage	V_{OUT}"1"	Fan-out ≦ 10 MOS Gate Loads V_{IN} = 0 V	9.99	10	-	V	
Noise Immunity: "1" Level Threshold Drain Current	$I_{D(TH)1}$	V_{IN} = 9 V	-	1	10	µA	3f
"0" Level Threshold Drain Current	$I_{D(TH)0}$	V_{IN} = 1 V	-	1	10	µA	3f
Noise Margin	V_{NM}	V_{IN} = V_{OUT}	3.3	4.5	6.7	V	3a
DC Input Current	I_{IN}	V_{IN} = 0 V	-	10	-	pA	
		V_{IN} = 10 V	-	10	-	pA	
Quiescent Device Dissipation Per Package	P/pkg	terminals: 7,4,9 = 0 V 14,2,11 = 10 V 1 to 5 8 to 13 inputs 3,6,10 = 0 V	-	0.01	1	µW	
		inputs 3,6,10 = 10 V	-	0.01	1	µW	
DC Drain-to-Source Current: "P" Inverter	I_{DS}	V_{GS} = -10 V, V_{DS} = -3 V	-2	-11.8	-	mA	5,6
		V_{GS} = -10 V, V_{DS} = -0.5 V	-1	-3.2	-	mA	5,6
"N" Inverter		V_{GS} = 10 V, V_{DS} = 3 V	2	5.4	-	mA	7,8
		V_{GS} = 10 V, V_{DS} = 0.5 V	1	1.5	-	mA	7,8
Input Capacitance (Average)	C_{IN}	each Input (terminals 3,6,10)	-	5	-	pF	20
CHARACTERISTICS FOR INDIVIDUAL "P" AND "N" MOS UNITS							
Switching Threshold Voltage: "P"-Unit	V_{TH}	V_{DS} = -10 V, I_D = -10 µA	-1	-3	-4	V	
"N"-Unit		V_{DS} = 10 V, I_D = 10 µA	1	2.5	4	V	
DC Forward Transconductance: "P"-Unit	g_{fs}	V_{GS} = -10 V, V_{DS} = -3 V	200	1000	-	µmho	
"N"-Unit		V_{GS} = 10 V, V_{DS} = 3 V	200	500	-	µmho	
Drain-to-Source Leakage Current: "P"-Unit	I_{DSS}	V_{GS} = 0 V, V_{DS} = -15 V	-	1	-	µA	
"N"-Unit		V_{GS} = 0 V, V_{DS} = 15 V	-	1	-	µA	
Drain-to-Source Breakdown Voltage: "P"-Unit	$V_{(BR)DS}$	V_{GS} = 0 V, I_D = -10 µA	-	20	-	V	
"N"-Unit		V_{GS} = 0 V, I_D = 10 µA	-	20	-	V	

DYNAMIC ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CD4007, CD4007D MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS FIGS.
"0" Propagation Delay (Inverter)	t_{pd0}	C_L = 50 pF	-	65	125	ns	15, 16
"1" Propagation Delay (Inverter)	t_{pd1}		-	65	125	ns	15, 17
"0" Transition Time (Inverter)	t_0		-	125	250	ns	15, 18
"1" Transition Time (Inverter)	t_1		-	125	250	ns	15, 19

Fig.3 - Transfer Characteristics.



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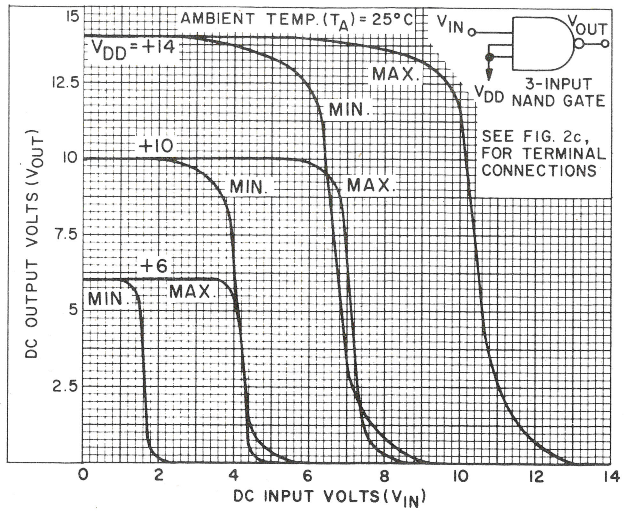
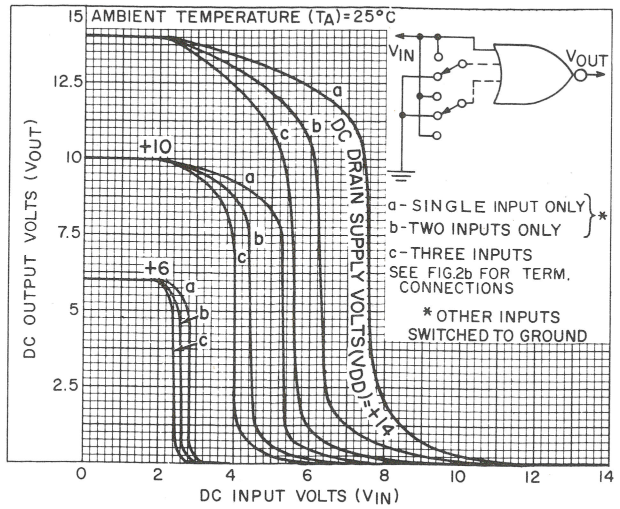
(a) minimum and maximum — inverter and NOR gate



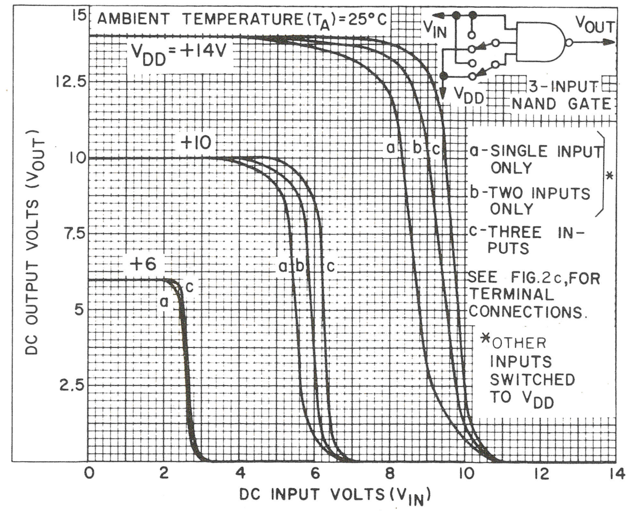
92CS-15305

(b) minimum and maximum — NAND gate



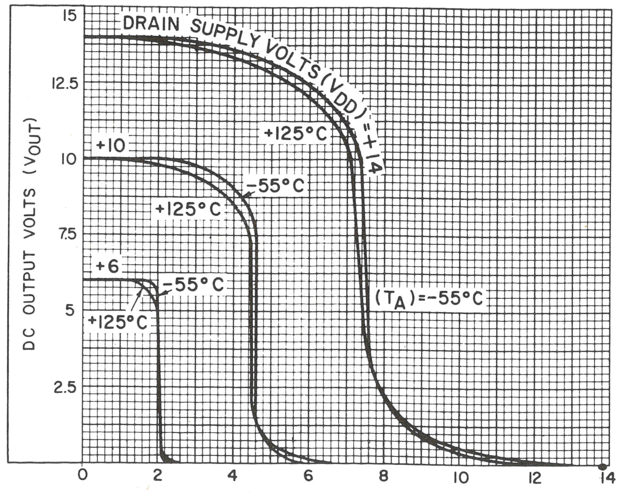
92CS-15326

(c) typical — NOR gate



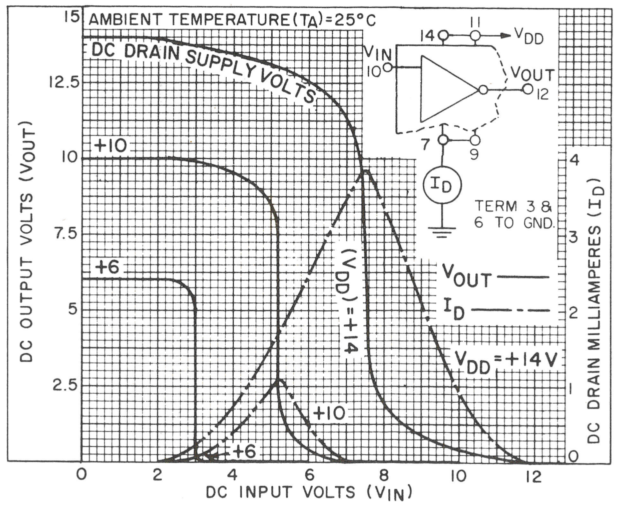
92CS-15306

(d) typical — NAND gate



92CS-15276

(e) typical transfer characteristics variations over temperature range (NAND, NOR, or inverter)



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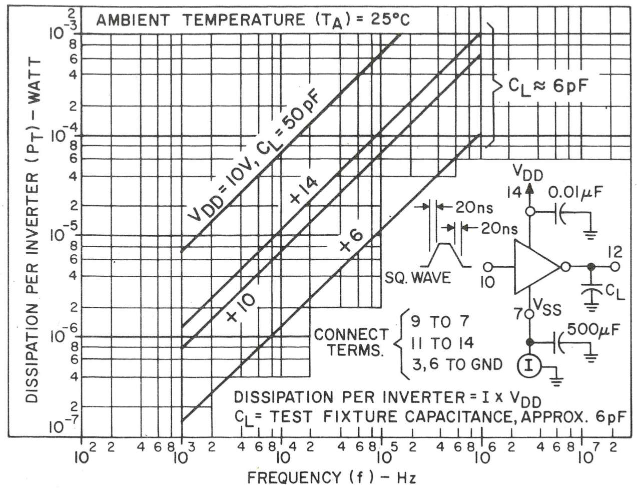
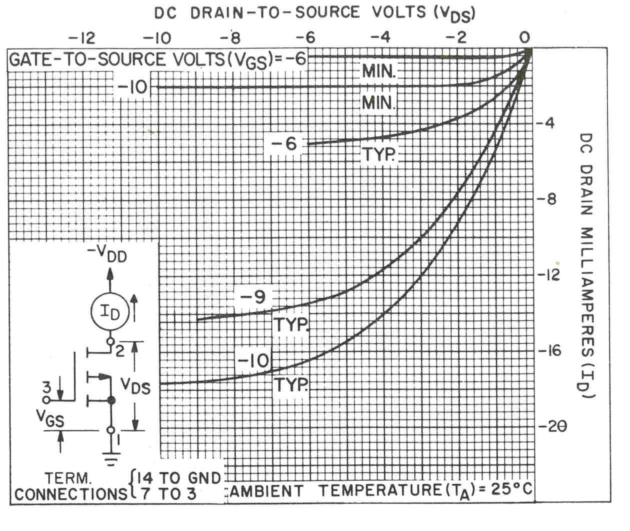
(f) typical current and voltage transfer characteristics



92CS-15320

Fig.4 - Typical Dissipation Characteristics.



92CS-15321

Fig.5 - Typical and Minimum P-Channel Drain Characteristics.

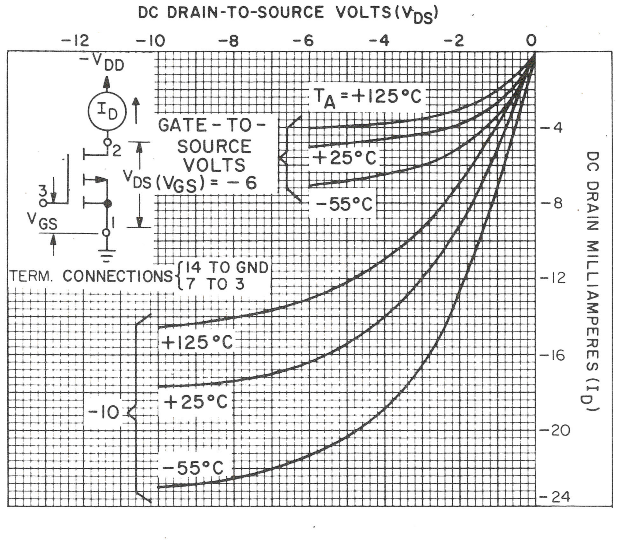


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Fig.6 - Typical P-Channel Drain Characteristics as a Function of Temperature.

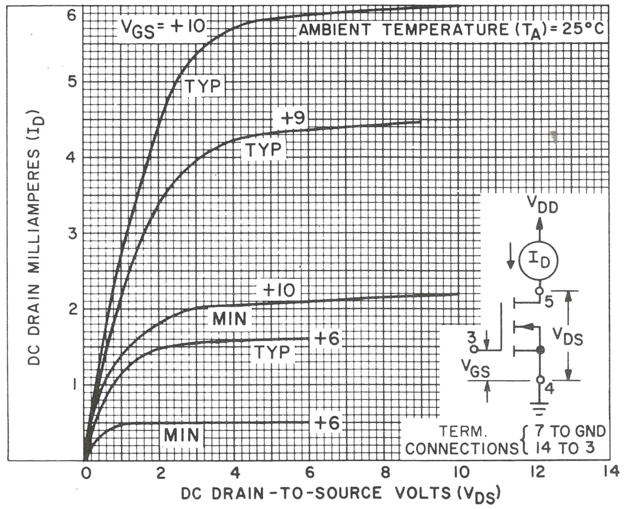

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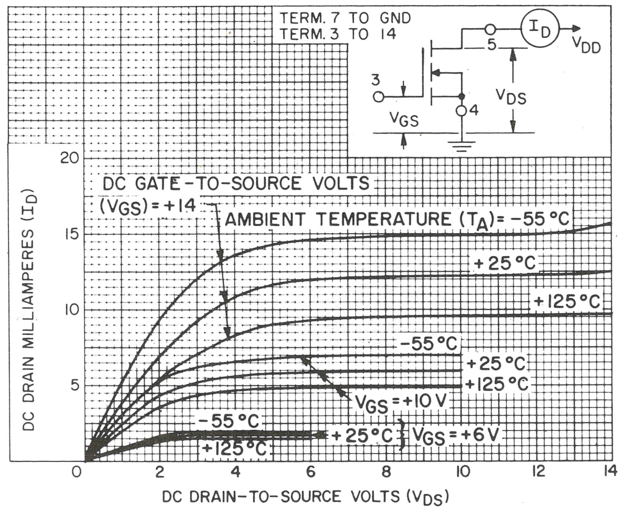
Fig.7 - Typical and Minimum N-Channel Drain Characteristics.



92CS-15324

Fig.8 - Typical N-Channel Drain Characteristics as a Function of Temperature.

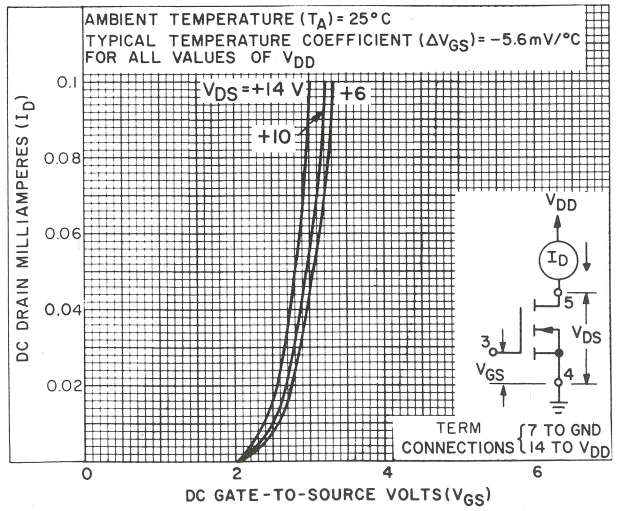


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Fig.9 - Typical N-Channel "Turn-On" Characteristics.

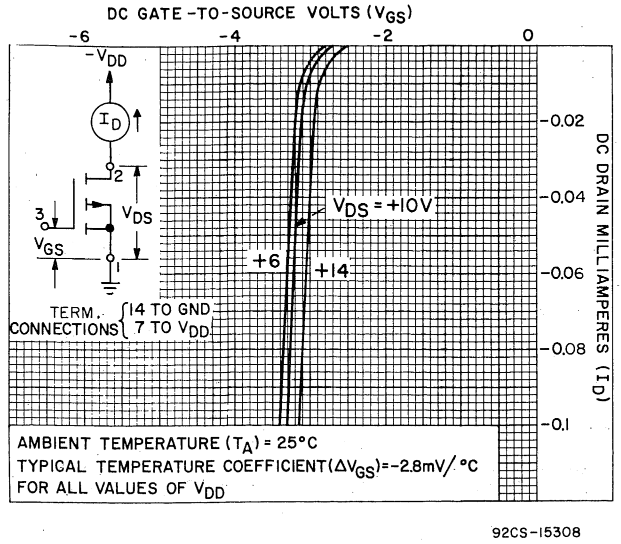


Fig.10 - Typical P-Channel "Turn-On" Characteristics.

TYPICAL CHARACTERISTICS MATCHING — Any Two Units on the Same Chip

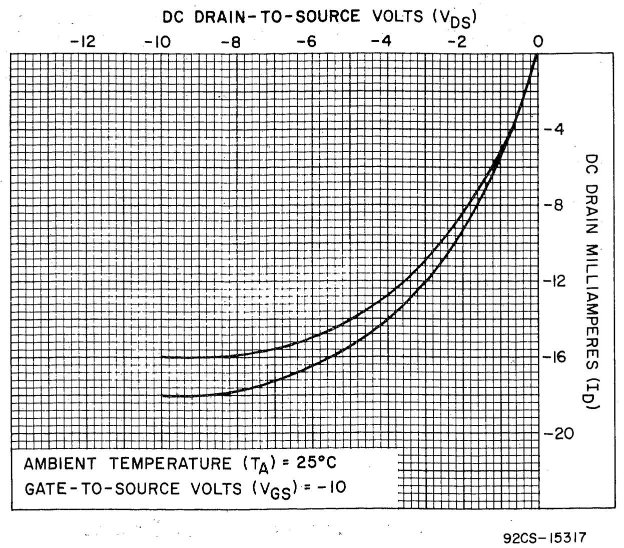


Fig.11 - P-Channel Drain Characteristics.

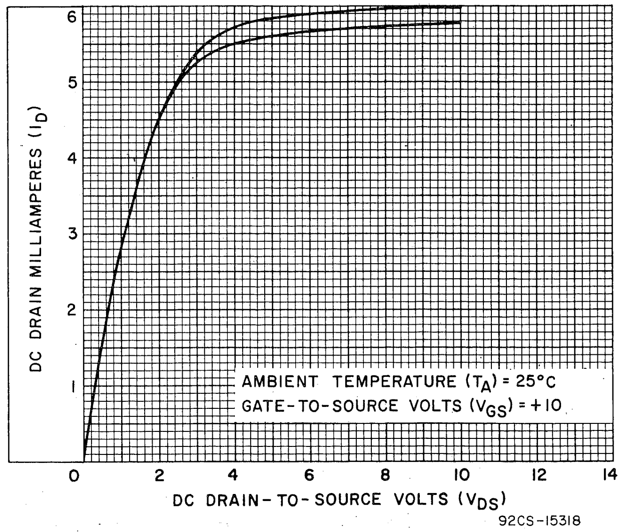


Fig.12 - N-Channel Drain Characteristics.

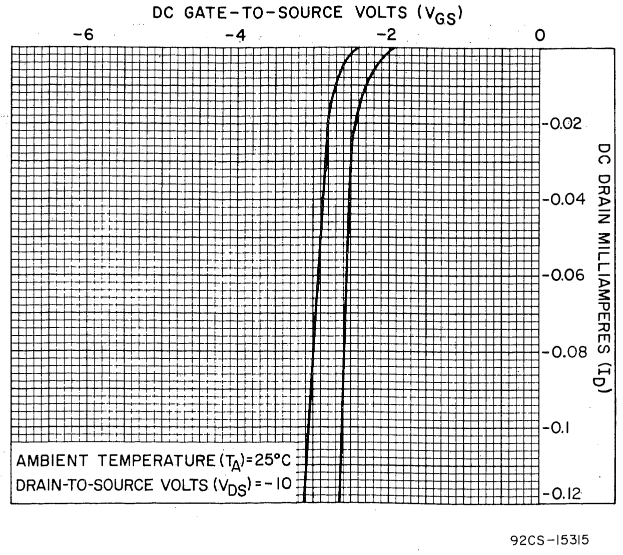


Fig.13 - P-Channel "Turn-On" Characteristics.

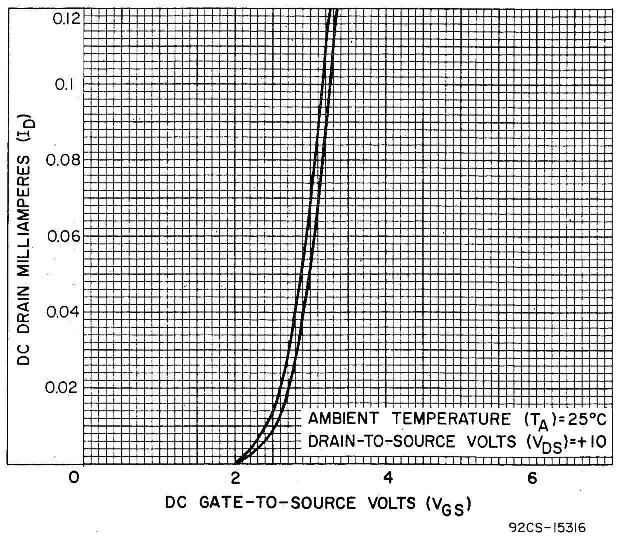


Fig.14 - N-Channel "Turn-On" Characteristics.

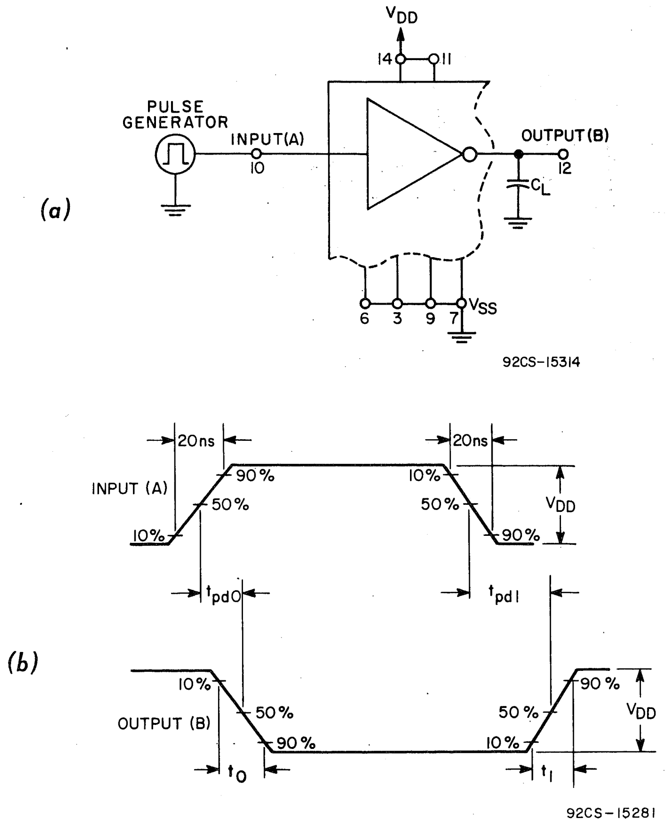


Fig.15 - Propagation Delay Test Setup (a) and Waveforms (b).

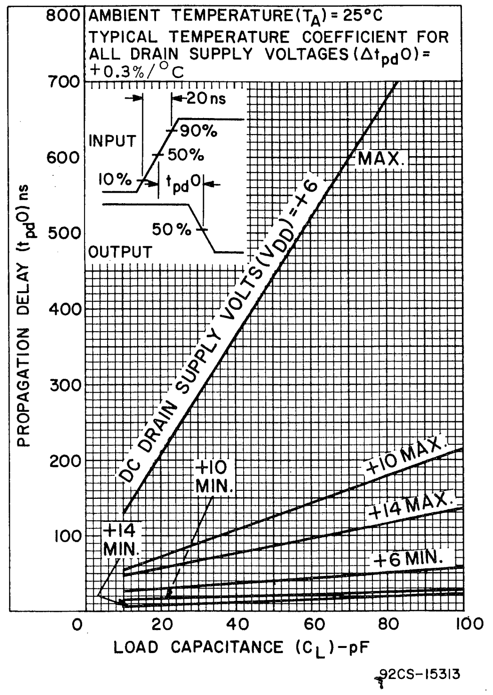


Fig.16 - Maximum and Minimum "Zero" Propagation Delay Characteristics.

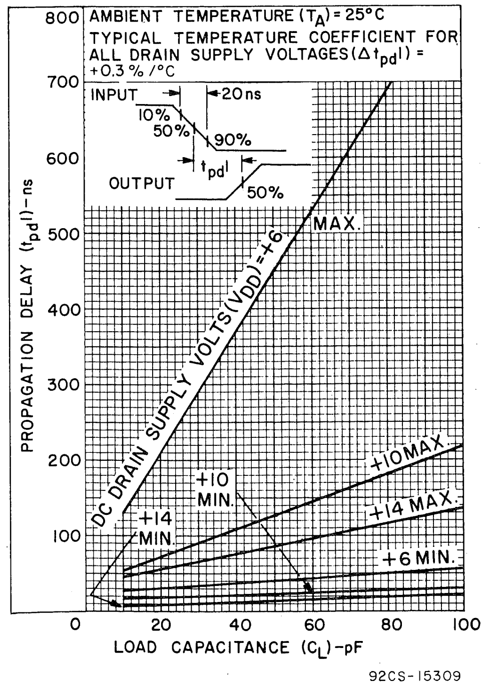


Fig.17 - Maximum and Minimum "One" Propagation Delay Characteristics.

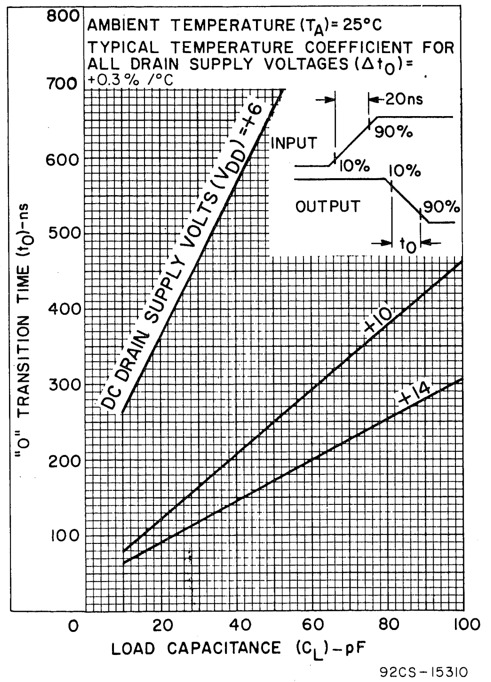


Fig.18 - Maximum "Zero" Transition Time Characteristics.

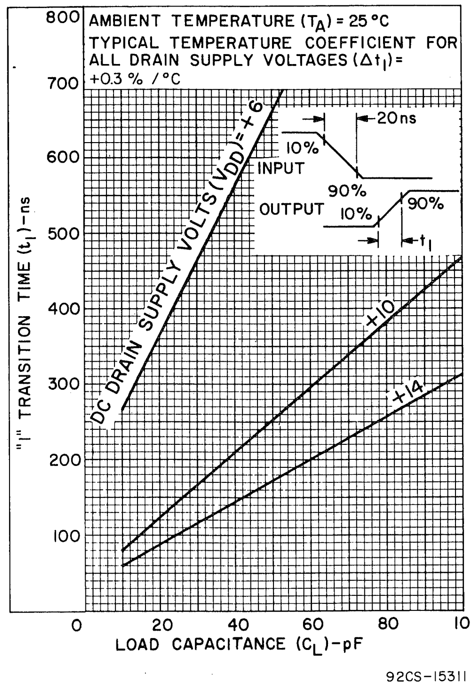


Fig.19 - Maximum "One" Transition Time Characteristics.

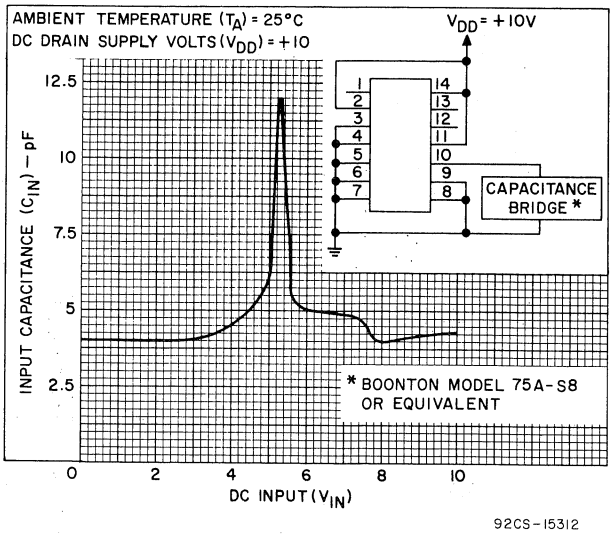


Fig.20 - Typical Input Capacitance Characteristic.

OPERATING CONSIDERATIONS

The leads of these devices are usually soldered to external circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields. Although a certain degree of protection against such fields is provided by built-in circuitry, it is recommended that this device not be inserted in conventional plastic "snow" or plastic trays of the types frequently used for the storage and transportation of small semiconductor devices.

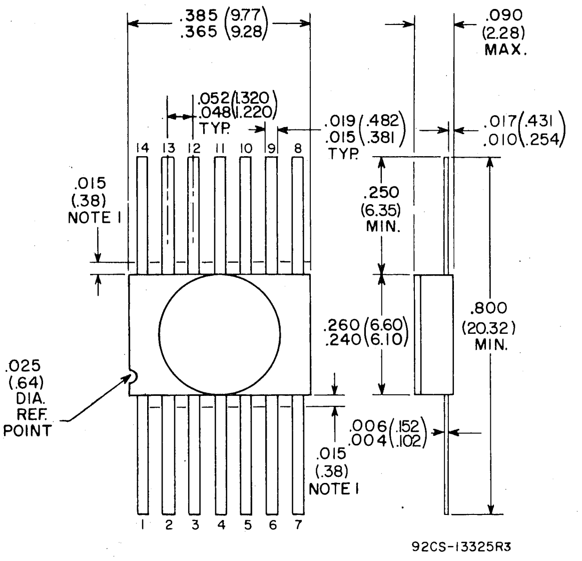
These units should not be connected into, or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device. All unused input leads should be connected to the most negative circuit potential. It is recommended that low impedance pulse generators or power supplies connected to the inputs of this device be removed before the power supply is turned off. This precaution will prevent the signal on the gate from exceeding the power supply voltage and thus, prevent possible damage to the protective circuitry.

DIMENSIONAL OUTLINES

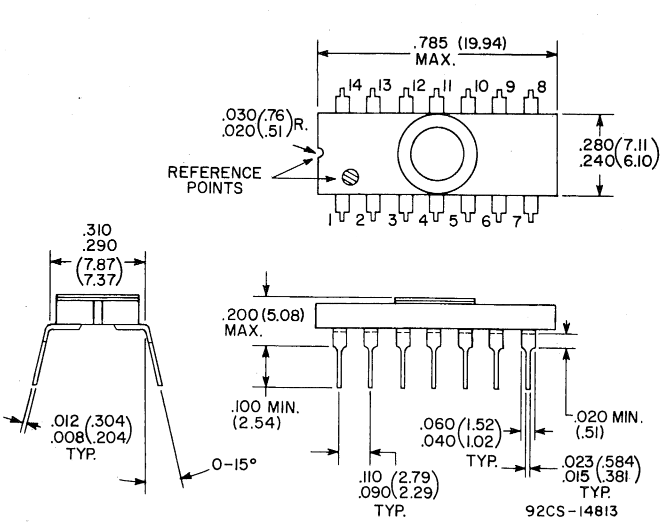
Dimensions in Inches and Millimeters

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated

CD4007



CD4007D



Note 1: Lead dimensions in this zone are not controlled because of irregularities in body and lead finish.

Lead spacing shall be measured within 0.030" (.762 mm) from the point of emergence from the body.